

# RF+ SiP Platform

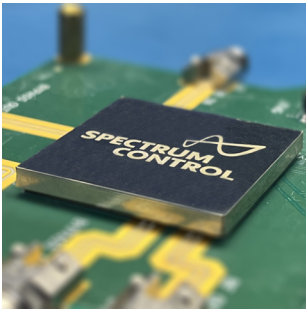
**System building blocks for modern RF+digital systems**

Complete platform for mixed signal integration in small surface-mount packages: high fidelity RF signal conditioning, power supply & distribution, and digital tuning, command & control.

- Miniature and integrated
- Software-instrumented
- Dramatically reduced cost and development time
- No performance trade-offs

# A Scalable, Flexible Platform for System Development

We are redefining how developers can design and build modern RF and digital systems with fully embedded, system-ready solutions.



- Radically shrink system footprint without compromising performance
- Significantly reduce engineering time with pre-engineered system blocks
- Profoundly simplify manufacturing and lower cost with volume-ready SMT solutions

Applications include wireless comms, test & measurement, and aerospace & defense.

## The Smarter Way to Build RF+Digital Systems

### Accelerated Design

Save thousands of engineering hours with pre-qualified, pre-tested SiPs that simplify your RF+Digital development. Simply plug and play into your system.

### Simplified Sourcing

We select, characterize, integrate and test the best components so you don't have to.

### Software-Instrumented for Embedded Control

FPGA-based control architecture enables software tuning, rapid integration, and performance stability across frequency ranges, all with minimal power draw. Ready for dynamic management by ML/AI.

### Integrated Power Management

Each SiP delivers unified power regulation, conversion, and routing, requiring only one or two low-voltage inputs.

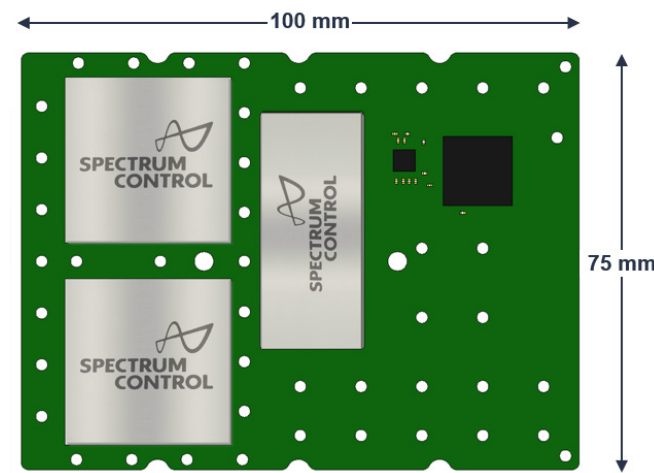
## Optimize Your Digital-Analog Integration

### Achieve optimal system performance

Combine the configurability of direct sampling with the speed and signal integrity of mission-specific analog front ends.

### Reduce design risk

Our SiP platform helps you avoid the integration challenges, interoperability issues, and latency penalties commonly associated with mixed-signal architectures.



Minimize board space and maximize performance with our compact SiPs.

## Improve the density of 3U VPX, VNX and other form factors

How will you shrink your 6G system footprint or use that extra board space to enhance the mission?

# SiP Platform Architecture



## Frequency Converter SiPs

High-fidelity millimeter wave block conversion in a high-volume package. Extend the frequency range of your existing 2-18 GHz system or design a new system that operates in the 18-40 GHz bands with

small footprint and high performance. These are single-channel (up or down) block converters that can be used separately or together for receive and/or transmit functions.

Ux1

Dx1

### Single-channel mmWave block converters

Extend the frequency range of your existing 2-18 GHz system or design a new system that operates in the 18-40 GHz bands with small footprint and high performance.

Ux2

Dx2

### Multi-channel mmWave block converters

Rapidly design a new multi-channel system that operates in the 18-40 GHz frequencies and then downconverts to IF in the 2-18 GHz frequency band for processing.

### Upconverter SiP

- 12 Voltage Regulators
- 12 RF Amplifiers
- 2 Digital Attenuators
- 3 RF Detectors
- 10 RF Filters

### Downconverter SiP

- 13 Voltage Regulators
- 11 RF Amplifiers
- 2 Digital Attenuators
- RF detector
- 11 RF Filters

These SiPs are offered in two configurations: standalone or multi-channel with a distributed control architecture.

## Service SiPs

These SiPs are designed to work in support of other SiPs to provide distributed control, high quality reference signals and more.

LOx4

4-channel local oscillator

CLx4

32 GHz Clock SiP for high-speed direct sampling

Ctrl

Central control SiP for multi-channel implementations

## Custom SiPs

Leverage our design, simulation, and manufacturing platform to produce high performance, ultra-small, surface-mount, integrated microwave assemblies (IMAs).

- Innovative material science and packaging technology
- Proven, repeatable miniaturization technology and processes
- Wideband and high frequency expertise
- Low NRE
- Rapid turnaround time from concept to production
- Cost-effective—designed for volume

### Custom SiP examples include

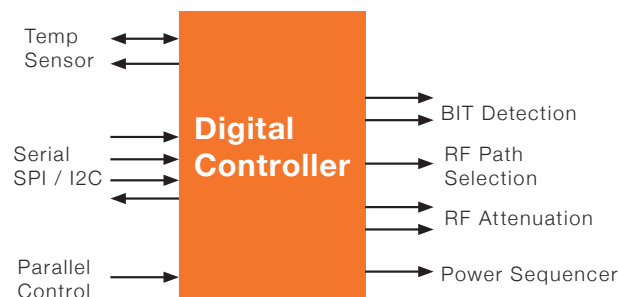
- Wideband RF Front End
- X-Band RF Front End
- Switched Filter Banks
- Frequency Converters
- Power Amplifiers



## Software-Instrumented for Superior Tuning and Control

Our full-featured SiPs offer a digital-ready interface for easy integration into your system. Use our embedded FPGA-based control architecture to build sophisticated configuration profiles to maintain device performance across wide frequency ranges and different signal attenuation requirements. ML /AI-ready.

## Embedded Digital Gateway



## Graphical User Interface

Master Control

nv5v SP Demo Instrument Control

Module Info

HW Part No: 273

HW Revision: 01

HW Serial No: 101

HW Data Code: 1224

FW Part No: 273

FW Revision: 05

SPB DIAG: PASS

IC2C DIAG: PASS

GPIO DIAG: PASS

Temperature: 23.625 C

Get Module Info

RF Path Select

☐ Band1
 ☐ Band2

Set RF Path

RF Switch Setting

BAND 1

Run Checkout

RF Attenuator Control

Input Attenuator: 0.0 dB  
 Output Attenuator: 0.0 dB

Set Attenuation

RF Attenuator Status

Input Attenuator: 31.5 dB  
 Output Attenuator: 16.0 dB

Power Sequencer Controls

Power Sequencer Control

☒ Sequencer Enable  
☐ Sequencer Disable

Power Sequencer Override

☐ Sequencer Override Enable  
☒ Sequencer Override Disable

5V Band 1 ON

5V Band 2 ON

5V Coremon ON

5V LO B1

5V LO B2

3.3V LO1

3.3V LO2

5V LO B1

5V LO B2

5V LO B1

5V LO B2

5V LO B1

5V LO B2

5V LO B1

5V LO B2

BIT Detection

RF Threshold: 0.000  
 SSI Threshold: 0.000  
☐ SSI Protect

Set Bit Threshold

Get Bit Status

Clear Bit Latch

Clear Max Hold

BIT Detect Status

RF Bit Threshold: 0.000  
 ADC Value: 0.005  
 ADC Max Hold: 0.010  
 Bit Latch:  
 SSI Threshold: 0.000  
 SSI Protection: 0

FAST Lookup Tables

Active State: 0

Write Values

RF Path:   
 Input Attenuator:   
 Output Attenuator:   
 RF Bit Threshold:

Set State Values

JTAG

Enable JTAG

Write Values

RF Path:   
 Input Attenuator:   
 Output Attenuator:   
 RF Bit Threshold:

Get State Values

COM Port

COM4

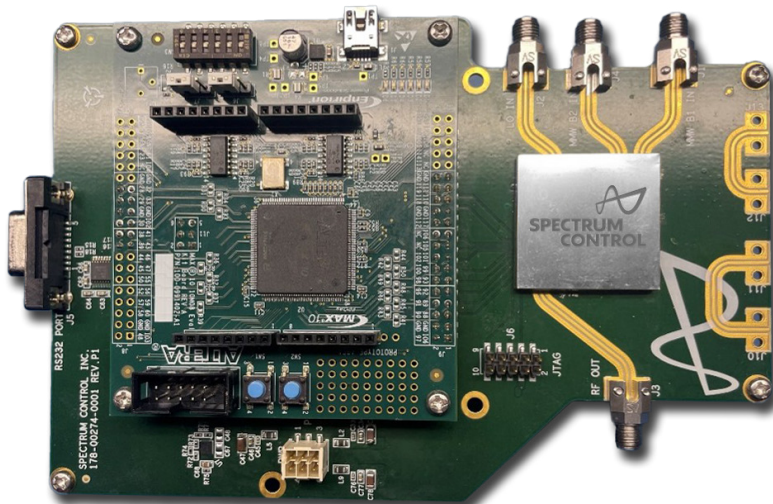
CONNECT

Run Checkout

Write: D0x0 DIO IO  
 Read: D0x0 DIO DIO Feedback Register  
 GPIO Feedback Passed!  
 Read: S0x0 Temperature Sensor  
 Read: D0x00 Temperature Register  
 Temperature: 23.625  
 Read: 0x1C from Power Sequencer Status Register  
 Read: D0x0 from RF Switch Path: Setting Register  
 Read: D0x0 from Input Attenuator Hardware Feedback Register  
 Read: D0x0 from RF Bit Threshold Register  
 Read: D0x0 from SSI Threshold Register  
 Read: D0x0 from RF Bit Latch Register  
 Read: D0x0 from SSI Threshold Register  
 Read: D0x0 from SSI Protect Enable Register  
 Enable Power Sequencer  
 Read: 0x1C from Power Sequencer Status Register  
 Enable Power Sequencer  
 Read: 0x1C from Power Sequencer Status Register  
 Enable Power Sequencer  
 Read: 0x1C from Power Sequencer Status Register  
 Enable Power Sequencer  
 Read: D0x10 from Power Sequencer Status Register  
 Write: D0x10 Power Sequencer Override  
 Read: D0x10 from Power Sequencer Status Register  
 Read: 0x1C from Power Sequencer Status Register  
 Enable Power Sequencer  
 Read: D0x0 from Power Sequencer Override Register  
 Read: D0x0 from Power Sequencer Status Register  
 Read: 0x1F from Power Sequencer Status Register  
 Write: D0x0 from RF Path Setting Register  
 Read: D0x0 from RF Switch Path: Setting Register

## Test Fixture/Evaluation Board

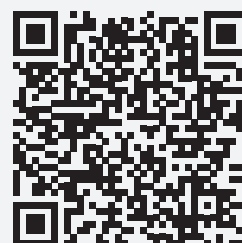
Put our SiPs to the test using our test fixture/evaluation board.



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